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Appl. No. 09/772,477

Amendment/Response

Reply to non-Final Office action of 21 May 2003

REMARKS/DISCUSSION OF ISSUES

Claims 1 through 8 are pending in the application.

The Examiner is respectfully requested to acknowledge the claim for priority and receipt of certified copies of all the priority document(s).

The Drawings are objected to in that Figs. 2 and 4-7 contain multiple figures which are not seperately labelled. Figs. 2 and 4-7 will be corrected to provide labels such as Fig. 2A, Fig. 2B, etc. for the separate figures, as shown in red on the enclosed prints of drawing sheets 1/4-4/4.

The Specification has been amended to conform the detailed description to the proposed drawing changes.

Claim 2 is rejected under 35 USC 112, first paragraph, as being unsupported by the Specification.

Claim 2 provides that the common luminance value data for the least significant subfields is obtained by averaging the corresponding least significant subfield original luminance values. Support for this language is clearly provided in the Specification in the paragraph beginning at line 25 of page 2, wherein it is stated:

According the invention, sets of adjacent lines (i.e. 2, 3 or more lines) are formed, and the same luminance value for some of the least significant subfields is displayed. By addressing more lines simultaneously, the address period is reduced, thereby leaving more time for the sustain period. The value displayed may be the average value of the original individual values. By grouping the lines differently in successive frames and/or different areas of the display, further reduction of the address period is obtained, without loss of resolution. (emphasis added).

The Examiner complains that the passage referred to above states only that the value displayed **may be** the average value. However, this language simply conveys that display of the

average value is an alternate embodiment, certainly a permissible and well-established technique for describing permissible variations of the invention.

Moreover, the Specification states in the paragraph beginning at line 9 of page 4:

A second improvement is obtained by displaying the average value of the original luminance value data of the set of lines, instead of a copy of one of the original lines to the other lines in the set, as is known in prior art document EP 0 890 941 for double line addressing.

Thus, the Specification makes clear that displaying the average value is a separate aspect of the invention.

The Examiner also states that there is no teaching of how to obtain the luminance value. However, there is no need for such a teaching, as it is well known in the art. See, for example, the discussion of Wani, EP 0 890 941, in the paragraph beginning at line 12 of page 1, under the section heading Background of the Invention.

Accordingly, it is felt that claim 2 is fully supported by the Specification, and it is urged that the rejection is in error and should be withdrawn.

Claims 1, 3, 5 and 8 are rejected under 35 USC 103(a) as being unpatentable over Wani (EP 0 890 941) in view of Kida et al.

Mani is cited by Applicant in the Background of the Invention, a portion of the discussion of which is referenced above. Wani teaches that the subfields representing the less significant bits, referred to as the lower four bits, are displayed by interlace scanning. This is a well known term of art, which means that every other line is scanned for one subfield, and the remaining lines are scanned for the next subfield. This interlaced scanning is explained by Applicant in C:\PROFESSIONAL\PhilipsAMDS2003\PHNLO00025amd.doc

terms of the odd low weight subfields b3, b1 being addressed to odd-numbered scanning lines and the even low weight subfields b4, b2 being addressed to even-numbered scanning lines. See page 2, lines 4-6 of Applicant's Specification.

In a second method taught by Wani, in which two lines are addressed simultaneously with the same data.

Both of these methods result in a loss of signal quality due to a loss of resolution and/or sharpness. See page 2, lines 12-16 of Applicant's Specification.

Applicant improves upon these methods by grouping the lines differently in successive frames and/or different areas of the display, resulting in the desired reduction of the address period without an accompanying loss of resolution. See page 2, lines 29-31 of Applicant's Specification.

The Examiner relies on Kida et al. to show the driving of two neighboring rows as one unit in a first field, and for shifting the rows in a second field.

Kida et al. is concerned with the problem of how to process two different kinds of display signals on a single plasma display panel, an interlaced scan NTSC television signal for moving images, and a non-interlaced (progressive) scan computer monitor signal for stationary images. Kida et al. solves this problem by converting the interlaced scan signal to a progressive scan signal. This is done by assigning the same luminance value to neighboring lines, and addressing these neighboring lines together as a unit. For each subsequent frame, the unit is moved to the next line. This technique reduces the address period by half and avoids the need to increase the frame memory. See, col. 7, lines 14-17.

Kida et al. makes no distinction between subfields having most or least significant bits. In fact, applying Kida et al.'s c:\PROFESSIONAL\PhilipsAMDS2003\PHNL000025amd.doc

technique to only some of the subfields would require an increase in the frame memory, and would not convert the interlaced scan signal to a progressive scan signal.

Thus, the skilled artisan would not be led by Kida et al. to drive neighboring rows of only some of the subfields, i.e., the lower four bits of the Wani signal, at the same luminance value, and accordingly the combination of Wani and Kida et al. fails to teach or suggest Applicant's claimed invention.

In order to make the distinction between Applicant's invention and Kida et al. more clear, claim 1 has been amended to call for the addressing to be applied to at least one of the least significant subfields.

Accordingly, claims 1, 3, 5 and 8 are not obvious in view of the combination of Wani in view of Kida et al., and the rejection is in error and should be withdrawn.

Claim 4 is rejected under 35 USC 103(a) over Wani in view of Kida et al. and further in view of Huang.

Without conceding the patentability per se of claim 4, it is urged that claim 4 is patentable by virtue of its dependency on claim 1, and that therefore the rejection is in error and should be withdrawn.

Claim 6 is rejected under 35 USC 103(a) over Wani in view of Kida et al. and further in view of Nagai.

Without conceding the patentability per se of claim 6, it is urged that claim 6 is patentable by virtue of its dependency on claim 1, and that therefore the rejection is in error and should be withdrawn.

Claim 7 is rejected under 35 USC 103(a) over Wani in view of Kida et al. and further in view of Prince et al.

Without conceding the patentability per se of claim 7, it is urged that claim 7 is patentable by virtue of its dependency c:\PROFESSIONAL\PhilipsAMDS2003\PHNL000025amd.doc

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on claim 1, and that therefore the rejection is in error and should be withdrawn.

In view of the foregoing, Applicant respectfully requests that the Examiner withdraw the rejections of record, allow all the pending claims, and find the application to be in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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Consulting Patent Attorney

203-329-6584



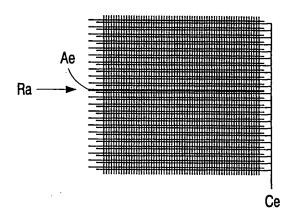


FIG. 1

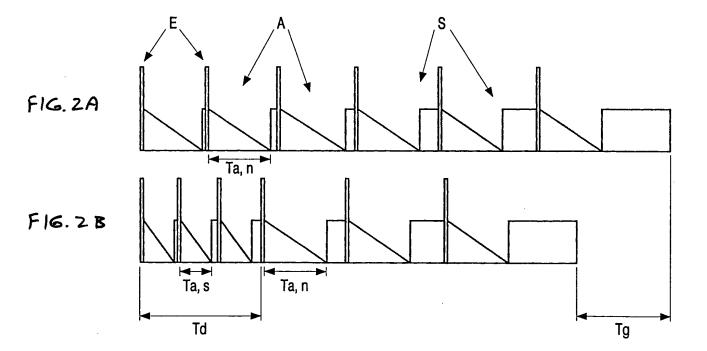


FIG. 2



2/4

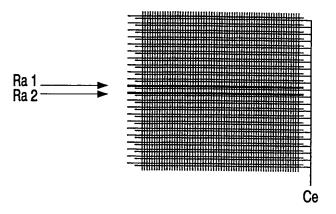
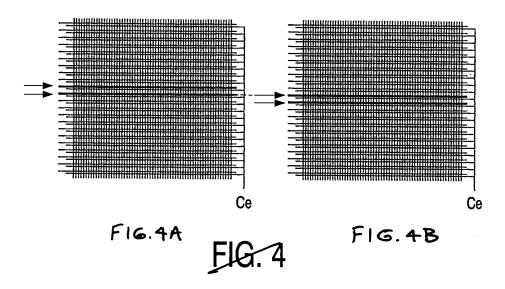
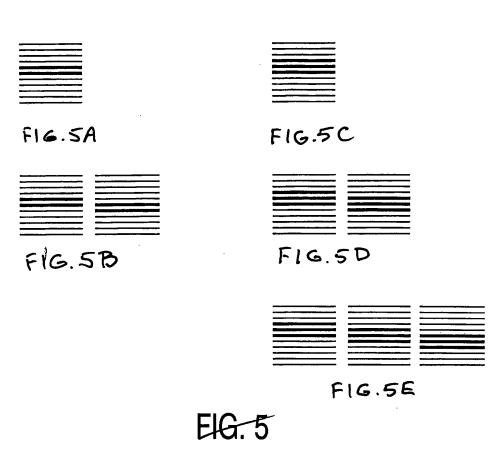


FIG. 3









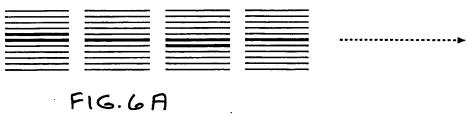
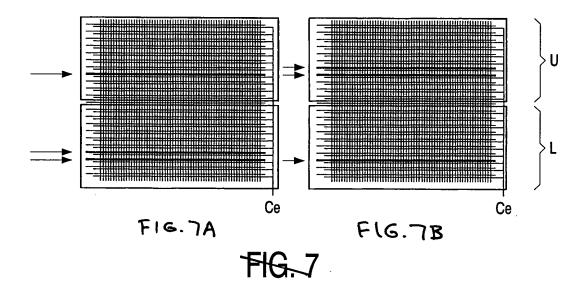




FIG. 6 B







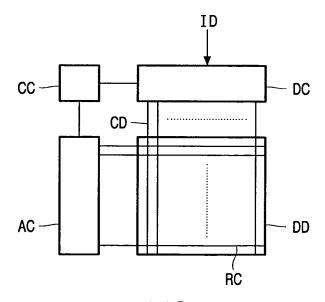


FIG. 8